

S/N 10/600,048

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Louis A. Lippincott	Examiner:	Hau Nguyen
Serial No.:	10/600,048	Group Art Unit:	2628
Filed:	June 19, 2003	Docket:	884.899US1
Title:	COMMUNICATION PORTS IN A DATA DRIVEN ARCHITECTURE		

REPLY BRIEF UNDER 37 C.F.R. § 41.41

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPELLANT'S REPLY BRIEF

This Reply Brief is filed in response to the Examiner's Answer (hereinafter, the "Answer"), mailed November 12, 2009, and supplements the Appeal Brief filed by the Appellant on April 17, 2009 and the Response to Notification of Non-Compliant Appeal Brief filed by the Appellant on August 4, 2009. Please charge any required additional fees or credit overpayments to Deposit Account 19-0743.

Argument

The Appellant has reviewed the Answer, and believes the statements in the Appeal Brief remain accurate and compelling. In responding to the Answer, the Appellant would like to further explore a selected few of the points raised by the Office in the Answer.

As argued in the Appeal Brief, the combination of Tulpule and Galicki fails to disclose "the second processor and the third processor are configured to establish a logical connection between the first processor and the second processor, the logical connection to originate at first processor and to traverse through the third processor and to complete at the second processor, wherein the logical connection is established *based on other active logical connections that include at least one of the first processor, the second processor and third processor*" (emphasis added). In response to Appellant's arguments, the Answer, at page 8-9, clarifies the Examiner's interpretation of Galicki by quoting Galicki at column 8, lines 48-56 as follows:

... During typical operation, data packets arriving to the receiver from the center port of the local bridge are packed into words and transferred to the

local I/O RAM at the current address of the active receive channel. There can be only one active channel at anyone time, so a packet that wants to deposit its data into a specific channel, should contain a CHAN rx_opcode in its header to activate the correct channel before the body of the packet reaches the receiver".

Thus according to the Answer:

If the first, second, or third processor is not the active received channels, data can exit the DSP through the left or right port, (see Fig. 6, col. 6, lines 43-55, i.e. depending on other logical connections). It is also noted that Galicki teaches broadcast packets can navigate to multiple destinations (col. 5, lines 48-62); that means more than one logical connections are established between the processors.

Appellant respectfully disagrees with this interpretation of Galicki. First, the mere presence of the physical connection of the ports of the processors fails to imply any logical connections are used to route data. Second, Galicki merely states that data "can exit through the left or right port." However, Galicki fails to disclose any methodology for choosing which port, the left port or the right port, is to be used for a logical connection. This is in contrast to the language recited in claim 1, in which the logical connection is established "based on other active logical connections that include at least one of the first processor, the second processor and third processor." Further, Galicki explicitly states at column 6, lines 43-55 that "[d]epending on the header evaluation, the point-to-point and cell packets may be routed out the bridge through left port 601, right port 602 or center port 603." Thus Galicki bases its determination of logical connections based on header information, not on active connections as recited in the claims.

As argued in the Appeal Brief, the combination of Tulpule and Galicki fails to teach at least "the source image signal processor is to transmit an initialize signal, prior to transmission of data along the logical connection, through the number of intermediate image signal processors to the destination image signal processor in the order that data is transmitted in the logical connection." In response to Appellant's arguments, the Answer, at pages 9-10, clarifies the Examiner's interpretation of Galicki, quoting column 8, lines 48-56 of Galicki as follows:

... a packet that wants to deposit its data into a specific channel, should contain a CHAN rx opcode in its header to activate the correct channel before the body of the packet reaches the receiver.

The Examiner thus interprets Galicki to teach that that "the headers [sic] is initialized and

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transmitted to the destination processor” and that the “header is then evaluated first at the destination processor prior to accepting the data.”

Appellant respectfully disagrees that the interpretation provided in the Answer teaches “the source image signal processor is to transmit an initialize signal, prior to transmission of data along the logical connection, through the number of intermediate image signal processors to the destination image signal processor in the order that data is transmitted in the logical connection” as recited in the claims. Appellant notes that the activities in the cited portion of Galicki appear to take place on a single processor. That is, the header analysis is performed on a transmitting processor prior to sending to a receiving processor. This activity fails to disclose anything related to transmission “through the number of intermediate image signal processors,” rather it describes activities that take place on a single processor that is preparing to transmit to a receiving processor.

Conclusion

In summary, for the reasons set forth above and in the Appeal Brief, the claims have been improperly rejected. Therefore, the Appellant respectfully requests that these rejections be reversed, with allowance of the pending claims.

Appellant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 373-6954 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Date January 12, 2009

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 12th day of January 2010.

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Signature